The Implementation of Vedic Algorithms in Digital Signal Processing*

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Digital signal processing (DSP) is the technology that is omnipresent in almost every engineering discipline. It is also the fastest growing technology this century and, therefore, it poses tremendous challenges to the engineering community. Faster additions and multiplications are of extreme importance in DSP for convolution, discrete Fourier transforms, digital filters, etc. The core computing process is always a multiplication routine; therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them. Vedic mathematics is the name given to the ancient system of mathematics, which was rediscovered, from the Vedas between 1911 and 1918 by Sri Bharati Krishna Tirthaji. The whole of Vedic mathematics is based on 16 *sutras* (word formulae) and manifests a unified structure of mathematics. As such, the methods are complementary, direct and easy. The authors highlight the use of multiplication process based on Vedic algorithms and its implementations on 8085 and 8086 microprocessors, resulting in appreciable savings in processing time. The exploration of Vedic algorithms in the DSP domain may prove to be extremely advantageous. Engineering institutions now seek to incorporate research-based studies in Vedic mathematics for its applications in various engineering processes. Further research prospects may include the design and development of a Vedic DSP chip using VLSI technology.

INTRODUCTION

Vedic mathematics is the name given to the ancient system of mathematics, or, to be precise, a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved – be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic *sutras* or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. Vedic mathematics was rediscovered from the ancient Indian scriptures between 1911 and 1918 by Sri Bharati Krishna Tirthaji (1884-1960), a scholar of Sanskrit, mathematics, history and philosophy [1]. He studied these ancient texts for years and, after careful investigation, was able to reconstruct a series of mathematical formulae called *sutras*.

Bharati Krishna Tirthaji, who was also the former Shankaracharya (major religious leader) of Puri, India, delved into the ancient Vedic texts and established the techniques of this system in his pioneering work, *Vedic Mathematics* (1965), which is considered the starting point for all work on Vedic mathematics. Vedic mathematics was immediately hailed as a new alternative system of mathematics when a copy of the book reached London in the late 1960s.

Some British mathematicians, including Kenneth Williams, Andrew Nicholas and Jeremy Pickles, took interest in this new system. They extended the introductory material of Bharati Krishna's book, and delivered lectures on it in London. In 1981, this was collated into a book entitled *Introductory Lectures on Vedic Mathematics* [2]. A few successive trips to India by Andrew Nicholas between 1981 and 1987

renewed interest in Vedic mathematics, and scholars and teachers in India started taking it seriously. According to Mahesh Yogi, *The* sutras *of Vedic Mathematics are the software for the cosmic computer that runs this universe*. A great deal of research is also being carried out on how to develop more powerful and easy applications of the Vedic *sutras* in geometry, calculus and computing.

Conventional mathematics is an integral part of engineering education since most engineering system designs are based on various mathematical approaches. All the leading manufacturers of microprocessors have developed their architectures to be suitable for conventional binary arithmetic methods. The need for faster processing speed is continuously driving major improvements in processor technologies, as well as the search for new algorithms. The Vedic mathematics approach is totally different and considered very close to the way a human mind works. A large amount of work has so far been done in understanding various methodologies (sutras). However, hardly any meaningful applications of Vedic algorithms have been thought of. In this article, the authors show how a successful attempt has been made to present two- and three-digit *multiplication* operations and the implementation of these using both conventional, as well as Vedic, mathematical methods in 8085/8086 microprocessor assembling language. The authors also highlight a comparative study of both approaches in terms of processing times (*T* states).

THE VEDIC MULTIPLICATION METHOD

The multiplication of two- or three-digit numbers utilising conventional mathematical methods (successive additions when used on computers) needs no explanation.

Alternatively, the Vedic method is illustrated in the example below. The digits on the two sides of line are multiplied and the result is added in the previous *carry*. When more than one line is in the step, all the results are added with the previous carry and the process is thus continued. Initially, the previous carry is equal to zero. A unit place digit of addition result is one of the digits in the answer; this is derived from full multiplication, while the remaining digits act as a carry. If the numbers of the digits are not same in the multiplier and multiplicand, then the bigger number has to be determined. The number of digits then needs to be counted. The smaller number should be pre-pended with 0s so that both numbers will be of the same digits [3].

The two digit multiplication example of 54 X 48 is given below.

Step 1:

carry=3

Step 2:

Step 3:

Three-digit multiplication (eg 532 X 438) is listed below.

Step 1:

Carry = 1

Step 2:

Step 3:

```
      5        3        2
X     4        3        8
   _____
         0    ·   1      6
```

Prev Carry = 3   new carry = 6
08
09
40
60

Step 4:

```
      5        3        2
X     4        3        8
   _____
         3    0    1     6
```
Prev carry = 6   new carry = 3
15
12
33

Step 5:

```
      5        3        2
X     4        3        8
   _____
      2  3   3   0   1   6
```

Prev Carry = 3
20
23
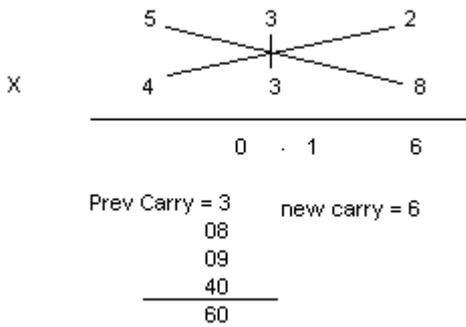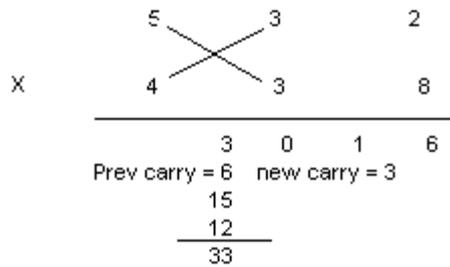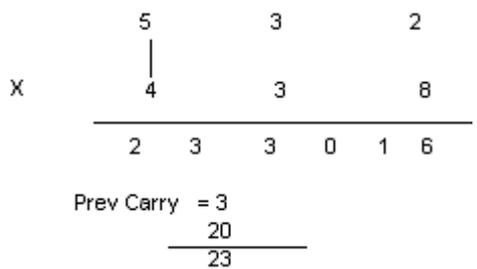
Answer: 532 * 438 = 233,016.

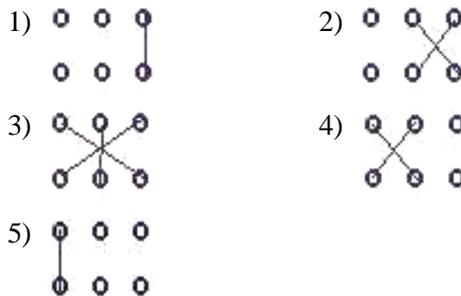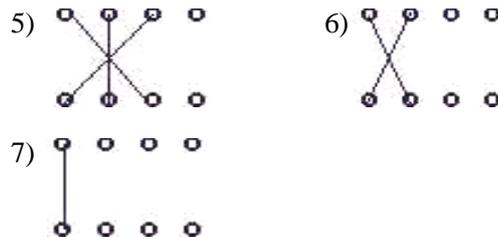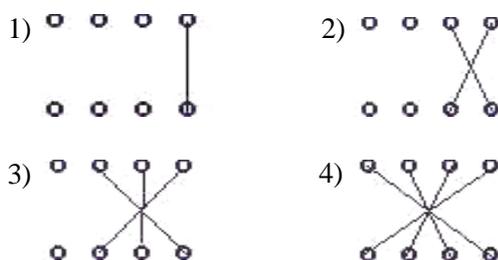For 3 digit numbers, the line diagram is represented as follows:

1)   2)
3)   4)
5)

The line diagram for four digits is given below:

1)   2)
3)   4)

5)   6)
7)

The flowchart for implementing Vedic multiplication in C language is listed in Figures 1 and 2.

COMPARATIVE STUDY OF PROCESSING TIMES OF CONVENTIONAL AND VEDIC MULTIPLICATIONS FOR 8085/8086 MICROPROCESSORS

By using the above-mentioned Vedic methods for two- and three-digit multiplications, assembly programs on 8085/8086 microprocessors were written, along with the number of clock states (T states) per instruction, in order to evaluate the total processing time for each of the methods [4].

Similar exercises have been completed for two- and three-digit multiplications utilising conventional mathematics methods. Both types of programs were successfully run to obtain the correct results (the assembly program listings could not be reproduced in this article due to paucity of space).

A 3 MHz clock used in 8085 Microprocessor gives one T state equal to 0.33 microseconds. Therefore, the total processing time is the product of total number of T states and the time period of one T state (ie 0.33 microseconds) [5]. A comparison of the processing times for Vedic and conventional mathematical methods in the case of two- and three-digit multiplications reveals the details listed below.

Two-digit multiplication yields the results shown in Table 1. As evidenced from Table 1, a time saving of approximately 59% can be achieved using the Vedic method.

Three-digit multiplication gives the results shown in Table 2.

In the case of three-digit multiplication, approximately 42% of the processing time is saved. Similar results can be obtained on other processors as well.

The above results are extremely encouraging so far as applications in digital signal processing (DSP) are concerned. Most of the important DSP algorithms, such as convolution, discrete Fourier transforms, fast Fourier transforms, digital filters, etc, incorporate *multiply-accumulate* computations [6]. Since the *multiplication* time is generally far greater than the *addition* time, the total processing time for any DSP algorithm primarily depends upon the number of multiplications. Therefore, the above-mentioned tabulated
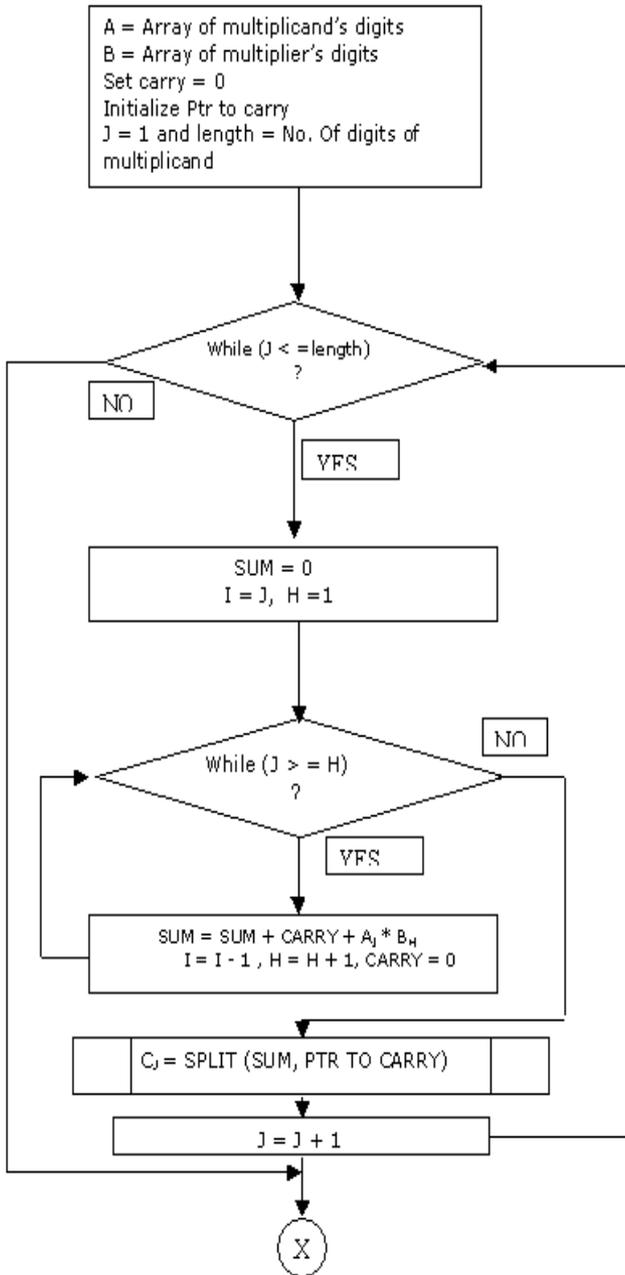
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Figure 1: Flowchart 1 for implementing Vedic multiplication in C language.

revelations indicate the overwhelming advantages of the Vedic approach.

The 8085/8086 microprocessors used thus far have standard INTEL architecture that is suitable for conventional mathematical methods. Even then, Vedic

Figure 2: Flowchart 2 for implementing Vedic multiplication in C language.

mathematical methods have achieved substantial time savings. If processor architectures that are convenient for Vedic methods are designed, then one can further reduce the processing time.

Since Vedic algorithms utilise decimal digits directly for their operations, it is considered appropriate to use

Table 1: Two-digit multiplication.

Method of multiplication	One T State in microsec.	Total No. of T States	Total Required Time (millisec.)
Conventional Method	0.33	2,417	0.810
Vedic Method	0.33	1,440	0.480

Table 2: Three-digit multiplication.

Method of multiplication	Time of One T State (microsec)	Total No. of T State	*Total Required Time (millisec)
Conventional Method	0.33	7,506	2.502
Vedic Method	0.33	3,128	1.042

binary coded decimal (BCD) architectures in place of the binary architecture presently used the world over. VLSI technology can provide the necessary design and simulation tools to develop processors based on BCD architecture. Such processors would be most suitable for implementing Vedic algorithms and may offer further savings in processing time.

CONCLUSIONS

Vedic mathematical methods are derived from ancient systems of computations, now made available to everyone through the great work of Jagadguru Swami Sri Bharati Krisna Tirthaji Maharaja, who published a book on Vedic mathematics in 1965. Compared to conventional mathematical methods, these are computationally faster and easy to perform.

The implementation of Vedic multiplication on 8085/ 8086 microprocessors and comparing it with conventional mathematics methods clearly indicates the computational advantages offered by Vedic methods. Therefore, such approaches are extremely beneficial in digital signal processing applications. There is an overwhelming need to explore Vedic algorithms in detail so as to verify its applicability in different domains of engineering.

Vedic algorithms implementations on specially designed BCD architecture will also help to enhance processor throughput.

An awareness of Vedic mathematics can be effectively increased if it is included in engineering education. In future, all the major universities may set up appropriate research centres to promote research works in Vedic mathematics.

ACKNOWLEDGEMENT

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BIOGRAPHIES

Prof. Purushottam D. Chidgupkar, Ex-Commander of the Indian Navy and post-graduate from Cranfield University, UK, has been at the MIT campus since January 1998. He has made noteworthy contributions in the development of one of the best IT infrastructure at the MIT Women Engineering College, Maha-rahstra Academy of Engineering and Educational Research, Pune, India. His own specialisation is in the area of digital signal processing (DSP) and has, to his credit, quite a few research projects completed under his close guidance.

He has also been exploring Vedic mathematics concepts for their usability in DSP. His research thus far has given ample evidence of the better efficiency of Vedic algorithms and their implementation in computers with reduced processing times. He intends to design separate processor architecture suitable for Vedic approaches and achieve further improvements in processing time.

Prof. Mangesh T. Karad is a postgraduate student in mechanical engineering at the MIT Women Engineering College, Maharahstra Academy of Engineering and Educational Research, Pune, India, having a long experience of teaching and guiding various projects at the undergraduate level. His area of specialisation has been *heat transfer* and has, to his credit, developed excellent teaching and learning models. He has presently been working as the Executive Director (Development and Planning) for the entire MIT Group of Institutions.

His most recent significant contribution to the MIT family has been the setting up of a fully-fledged Marine Engineering College (MANET) at the sprawling campus near Pune. He has also shown a keen interest in the development of Vedic mathematics for engineering applications and its integration into engineering education.

Conference Proceedings of the
7th UICEE Annual Conference on Engineering Education
under the theme: *Educating for the Global Community*

edited by Zenon J. Pudlowski

The *7th UICEE Annual Conference on Engineering Education*, held under the theme of *Educating for the Global Community*, was organised by the UNESCO International Centre for Engineering Education (UICEE) and was staged in Mumbai, Maharashtra State, India, between 9 and 13 February 2004.

This volume of Proceedings includes papers submitted to this Conference and offers a diverse compendium of articles that detail various international approaches to engineering education research and development related to the Conference theme, as well as other specific activities.

The 47 published papers, representing 21 countries, offer an excellent collection of works that tackle fundamental issues, concepts and achievements of individual researchers, as well as the concerns and challenges regarding engineering and technology education in different cultures.

The papers have been organised into the following groups:

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- Quality issues and improvements in engineering education
- Innovation and alternatives in engineering education
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This is no longer true and Professor Blackledge's book Digital Signal Processing will enable many people to make use of their interest in, and perhaps fascination with, mathematics in such a way, and through a eld of study, that will help us all communicate our ideas more quickly and conveniently through the digital world of today. vi. Preface to the Second Edition. This book provides an account of the mathematical background, computational meth-ods and software engineering associated with digital signal processing. The aim has been to provide the reader with the mathematical Digital signal processing (DSP) is the use of digital processing, such as by computers or more specialized digital signal processors, to perform a wide variety of signal processing operations. The signals processed in this manner are a sequence of numbers that represent samples of a continuous variable in a domain such as time, space, or frequency. Digital signal processing and analog signal processing are subfields of signal processing. DSP applications include audio and speech processing, sonar Digital signal processing is fastest growing area with large number of challenges in front of engineering community. Faster addition, multiplication, convolution, DFT implementation are very important. Core computing process is a multiplication process and there is a need to find out new faster algorithms and hardware implementation routines. The implementation of Vedic algorithms in the DSP domain may prove to be extremely advantageous. The implementation of Vedic multiplication on 8085/8086 microprocessors and comparing it with conventional mathematical methods clearly indicates the computational advantages offered by Vedic methods. Fast multiplication is very important in DSPs for operations like convolution and Fourier transforms.