

Erschienenene Publikationen Published Papers

(1) **Distribution and Properties of Oxide Precipitates in Annealed Nitrogen-doped 300 mm Si Wafers**

V.D. Akhmetov, H. Richter, W. Seifert, O. Lysytskiy, R. Wahlich, T. Müller, M. Reiche
European Journal of Applied Physics **27**, 159 (2004)

Spatial distribution and properties of oxide were examined in 300 mm nitrogen (N) doped CZ-Si. Experimentally grown materials with N ranging from 10^{13} cm^{-3} to 10^{15} cm^{-3} were studied by infrared light scattering tomography, scanning infrared microscopy, transmission electron microscopy and electron beam induced current. It was established that an increasing N content improves the uniformity of the radial distribution of precipitates in the bulk of the wafer, the density of precipitates reaching a level of 10^9 cm^{-3} . The width of the denuded zone varies in the range from 15 μm to 70 μm depending on radial position and N doping level. Electron microscopy revealed lower oxide precipitate densities of about 10^5 to 10^8 cm^{-3} . The results are interpreted in terms of existence of agglomerates of nanometer size precipitate nuclei and/or by the defect-induced strain relaxation around the precipitates.

(2) **Effects of Various Ci/Ti and Co/TiN Layer Stacks and the Silicide Rapid Thermal Process Conditions on Cobalt Silicide Formation**

S. Buschbaum, O. Fursenko, D. Bolze, D. Wolansky, V. Melnik, J. Nieß, W. Lerch
Microelectronic Engineering **76**, 311 (2004)

The effects of cap layer type (Ti or TiN) and its thickness, Co thickness and rapid thermal processing (RTP) temperature on cobalt silicide formation are investigated by a combination of electrical and optical measurements. Various Co/TiN and Co/Ti layer stacks (thicknesses 8-20 nm per layer) were deposited on (100) Si substrates. The first RTP step (RTP1) was performed by isochronal annealing at various temperatures between 400 and 600°C for 30 s. It was observed that the temperature range for constant sheet resistance (R_s) values after the first RTP step (RTP1 process window) is smaller for the Co/TiN layer stacks than it

is for the Co/Ti layer stacks. After the subsequent selective etch step the second RTP step (RTP2) was performed at 800°C for 30 s. R_s after RTP2 strongly depends on the initial Co thickness and its uniformity for both systems if the RTP1 temperature was above 470°C. For the Co/TiN layer stacks the final R_s results are not influenced by the RTP1 temperature or its uniformity (above 470°C). In this case silicidation is independent of the cap thickness. However, in the Co/Ti system the reactive Ti influences the silicidation process by reducing the amount of available Co in a manner that depends on the RTP1 temperature and the Ti cap thickness.

(3) **Aluminum Gettering in Photovoltaic Silicon**

J. Chen, D. Yang, X. Wang, D. Que, M. Kittler
European Physical Journal of Applied Physics **27**, 119 (2004)

The effect of aluminum gettering on different silicon materials used for solar cells has been investigated by means of microwave photoconductivity decay (μ -PCD) and electron beam induced current (EBIC). μ -PCD measurement revealed that the lifetime of multicrystalline silicon (mc-Si) with a lower initial lifetime could be increased by high temperature gettering (1000°C), while that of mc-Si with a higher initial lifetime could not be increased, but was even degraded. EBIC results revealed that no significant improvement of diffusion length was observed in both contaminated and uncontaminated wafers, while 850°C Al gettering was employed. It is concluded that both the initial material quality and the thermal treatment have influences on the effect of Al gettering. In addition, dislocations with bright EBIC contrast were discovered in annealed mc-Si wafers, the origin of which is discussed.

(4) **Assessing the Performance of Two-Dimensional Dopant Profiling Techniques**

N. Duhayon, P. Eyben, M. Fouchier, T. Clarysse, W. Vandervorst, D. Alvarez, S. Schoemann, M. Ciappa, M. Stangoni, W. Fichtner, P. Formanek, M. Kittler, V. Raineri, F. Giannazzo, D. Goghero, Y. Rosenwaks, R. Shikler, S. Saraf, S. Sadewasser, N. Barreau, T. Glatzel, M. Verheijen, S.A.M. Mentink, M. von Sprekelsen, T. Maltezopoulos, R. Wiesendanger, L. Hellemans
Journal of Vacuum Science & Technology **B 22** (1), 385 (2004)

This article discusses the results obtained from an extensive comparison set up between nine different European laboratories using different two-dimensional (2D) dopant profiling techniques (SCM, SSRM, KPFM, SEM, and electron holography). This study was done within the framework of a European project (HERCULAS), which is focused on the improvement of 2D-profiling tools. Different structures (staircase calibration samples, bipolar transistor, junctions) were used. By comparing the results for the different techniques, more insight is achieved into their strong and weak points and progress is made for each of these techniques concerning sample preparation, dynamic range, junction delineation, modeling, and quantification. Similar results were achieved for similar techniques. However, when comparing the results achieved with different techniques differences are noted.

(5) Electron Holography on Silicon Microstructures: A Comparison with Scanning Probe Techniques

P. Formanek, M. Kittler

Journal of Physics: Condensed Matter **16**, 193 (2004)

Two-dimensional dopant profiling is being strongly demanded by the semiconductor industry, and several techniques have been developed in recent years. We compare the performance of electron holography in a transmission electron microscope with other microscopic techniques. The advantages of electron holography are the high spatial resolution of a few nanometres and the direct interpretability of the measured two-dimensional electrostatic potential requiring no simulation. We demonstrate the detection of a 0.5 monolayer of boron in silicon and silicon germanium. We image a 35 nm wide potential dip of 25 mV in a boron-doped specimen, corresponding to detection of a $2 \times 10^{17} \text{ B cm}^{-3}$ dip between peaks of $2 \times 10^{18} \text{ B cm}^{-3}$. Moreover, we illustrate directly by electron holography the existence of a potential barrier at NiSi_2 precipitates in silicon, which was predicted earlier by the electron-beam-induced current technique.

(6) Development of Spectroscopic Ellipsometry as in-line Control for Co SALICIDE Process

O. Fursenko, J. Bauer, A. Goryachko, D. Bolze, P. Zaumseil, D. Krüger, D. Wolansky, E. Bugiel, B. Tillack

Thin Solid Films **450**, 248 (2004)

This work is aimed at in-line thickness and composition analysis of Co silicides by spectroscopic ellipsometry (SE). The silicides were formed by a two-step rapid thermal annealing (RTA) in nitrogen at different temperatures from initial Co layers deposited on Si (100) substrates and capped by a protective layer of TiN. The optical constants of Co, CoSi and CoSi films were calculated in the wavelength range of 240 x 800 nm, describing the optical dispersions by harmonic oscillator models. These models were applied for in-line thickness and composition control of the main steps of Co SALICIDE process. The effects of the first RTA temperature and initial Co thickness on formation of silicide phases and their thickness were evaluated. For phase identification, additional methods (sheet resistance, Auger electron spectroscopy and X-ray diffraction) were used. Finally, the suitability of SE for layer thickness uniformity evaluation was demonstrated for the main steps of Co SALICIDE process.

(7) Raman Investigation of Stress and Phase Transformation Induced in Silicon by Indentation at High Temperatures

S. Kouteva-Arguirova, V. Orlov, W. Seifert, J. Reif, H. Richter

European Physics Journal – Applied Physics **27** (1-3), 279 (2004)

To study the material deterioration at and around the support contacts during processing of silicon wafers, we used Rockwell indentation at elevated temperatures as a model. Cz-silicon was subjected for 30 s to a load of 1.5 N, at temperatures between 70°C and 660°C. The resulting morphology was checked by scanning electron microscopy. Micro Raman spectroscopy was used to monitor residual stress and the occurrence of silicon polymorphs. We found strong compressive stress inside the indented area, with a dramatic drop and reversal to tensile stress at its boundary. The morphology shows a top hat profile, covered with a mesh of vein-like structures. Crystalline phases such as Si-III, Si-IV, Si-XII, and amorphous silicon are observed. Outside the spot, the situation depends strongly on the indentation temperature. Up to 400°C the material appears practically unstressed, with a high density of relaxation cracks. At 500°C and 600°C a transition is found from strong tensile stress at the boundary to another region of compressive stress extending over more than 40 μm , associated with a significantly lower crack density. At still higher temperature (660°C)

the crack density tends to zero, and comparably weak stress seams to oscillate between compressive and tensile.

(8) Baseband Processor for IEEE 802.11a Standard with embedded BIST

M. Krstic, K. Maharatna, A. Troya, E. Grass, U. Jagdhold
Facta Universitatis, Series: Electronics and Energetics **17**, 231 (2004)

In this paper results of an IEEE 802.11a compliant low-power baseband processor implementation are presented. The detailed structure of the baseband processor and its constituent blocks is given. A design for testability strategy based on Built-In Self-Test (BIST) is proposed. Finally, implementational results and power estimation are reported.

(9) Characterization of Ge Gradients in SiGe HBTs by AES Depth Profile Simulation

D. Krüger, A. Penkov, Y. Yamamoto, A. Goryachko, B. Tillack
Applied Surface Science **224** (1-4), 51 (2004)

We show that AES depth profiling extended by a simple profile simulation technique allows characterization of details in the Ge concentration gradients for SiGe hetero-bipolar transistors (HBTs). Using the mixing-roughness-information depth (MRI) model to simulate the experimental data allows us to reveal concentration steps with a precision of about ± 2 at.% and small deviations from linear concentration gradients. The obtainable high lateral resolution of AES facilitates an application for process optimization and control in small microelectronic structures.

(10) Diffusion and Segregation of Shallow As and Sb Junctions in Silicon

D. Krüger, H. Rücker, B. Heinemann, V. Melnik, R. Kurps, D. Bolze
Journal of Vacuum Science and Technology **22** (1), 455 (2004)

The diffusion and segregation of Sb and As is investigated after low-energy implantation and annealing, both rapid thermal processing and furnace annealing. We demonstrate that the absence of transient enhanced diffusion effects for Sb facilitates the fabrication of significantly shallower junctions with less dopant se-

gregation to the surface. It is shown that Sb implantation can be used to fabricate low-resistivity ultrashallow junctions suitable for source/drain extensions in n-type metal-oxide-semiconductor field effect transistors.

(11) Oxide Formation During Ion Bombardement of Small Silicon Structures

D. Krüger, P. Formanek, E. Pippel, J. Woltersdorf, E. Bugiel, R. Kurps, G. Weidner
Journal of Vacuum Science and Technology **B 22** (3), 1179 (2004)

The kinetics of high dose oxygen implantation and of surface sputtering in silicon are investigated by atomic force microscopy, transmission electron microscopy, transmission electron holography, and electron energy-loss spectroscopy. The implantation was performed into accurately defined submicrometer areas. The behavior of the erosion rate as a function of the implantation dose proved to be nonmonotonic. After native oxide sputtering, a period dominated by (i) implantation of oxygen and (ii) induced oxide formation with volume increase takes place, causing a maximum surface step around the bombarded area of about 1.1 to 1.3 nm at bombardment doses below $2 \times 10^{16} \text{ O}^+ \text{ cm}^{-2}$. Subsequently, higher doses cause a sputtering of the surface with a sputter yield of about 0.32 Si atoms/ O^+ . Electron holography revealed the double layer character of the implanted region, and electron energy-loss spectroscopy, especially near the relevant Si-L23 ionization edge, identified these two layers which are (i) amorphous silicon oxide and (ii) amorphized silicon. Electron energy-loss line scans show the oxygen distribution inside the implanted areas with a lateral resolution of about 1-2 nm. It was found that the interface between the oxidized layer and the amorphized silicon sharpens with increasing implantation dose.

(12) Some Open Issues on Internetworking for the Next Generation

P. Langendörfer, V. Tsaoussidis
Computer Communications **27** (10), 908 (2004)

In this survey we focus on open issues of the wireless Internet. Our main intention is to elaborate what has to be done to integrate mobile devices in the Internet in such way that users do not experience any difference between wireless and fixed connections. We concentrate on the layers on top of IP, i.e. transport protocols, middleware platforms and applications. We pro-

vide an overview of existing solutions and a discussion of open issues and promising research directions is given for each of these fields.

(13) Solid State Reaction between Pr and SiO₂ Studied by Photoelectron Spectroscopy and ab initio Calculations

G. Lupina, J. Dabrowski, P. Formanek, D. Schmeißer, R. Sorge, C. Wenger, P. Zaumseil, H.-J. Müssig
Materials Science in Semiconductor Processing **7** (4-6), 215 (2004)

We report on the structural and electrical properties of Pr-based high-*k* dielectric films fabricated by solid-state reaction between metallic Pr and SiO₂ underlayers. A non-destructive depth profiling using synchrotron radiation excited photoelectron spectroscopy (SR-PES), X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) were employed to examine the chemical composition and microstructure. Ab initio calculations were done to gain insight into the physical processes involved. SR-PES results indicate that Pr deposition at room temperature (RT) leads to the formation of a Pr silicide and a Pr oxide, what is in good agreement with the scenario expected from ab initio calculations. As revealed by TEM and electrical measurements, oxidation of the reacted structures, followed by annealing, results in a stacked dielectric composed of a SiO₂-based buffer with an enhanced permittivity and a Pr silicate film with a high dielectric constant. The leakage current density of 10⁻⁴ A/cm² was measured for stacks with capacitance equivalent thickness (CET) of 1.5 nm prepared by evaporation of the Pr layer on a 1.8 nm SiO₂ film, followed by oxidation in air ambient and annealing in N₂ atmosphere. The capacitance-voltage (*C-V*) curves exhibit a large flatband voltage (*V_{FB}*) shift indicating the presence of a positive charge in the stack. Switching away from the Al contacts to Au gate electrodes introduces a significant reduction of the *V_{FB}* by 1.3 eV, what is much more than the change expected from the work function difference between Al and Au (~0.9 eV). This in turn implies that *V_{FB}* is strongly affected by the gate interface electrode.

(14) A 64-Point Fourier Transform Chip for High Speed Wireless LAN Application Using OFDM

K. Maharatna, E. Grass, U. Jagdhold
IEEE Journal of Solid State Circuits **39** (3), 484 (2004)

In this paper, we present a novel fixed-point 16-bit word-width 64-point FFT/IFFT processor developed primarily for the application in an OFDM-based IEEE 802.11a wireless LAN baseband processor. The 64-point FFT is realized by decomposing it into a two-dimensional structure of 8-point FFTs. This approach reduces the number of required complex multiplications compared to the conventional radix-2 64-point FFT algorithm. The complex multiplication operations are realized using shift-and-add operations. Thus, the processor does not use a two-input digital multiplier. It also does not need any RAM or ROM for internal storage of coefficients. The proposed 64-point FFT/IFFT processor has been fabricated and tested successfully using our in-house 0.25-µm BiCMOS technology. The core area of this chip is 6.8 mm². The average dynamic power consumption is 41 mW at 20 MHz operating frequency and 1.8 V supply voltage. The processor completes one parallel-to-parallel (i.e., when all input data are available in parallel and all output data are generated in parallel) 64-point FFT computation in 23 cycles. These features show that though it has been developed primarily for application in the IEEE 802.11a standard, it can be used for any application that requires fast operation as well as low power consumption.

(15) Fast Nondestructive Technique to Determine the Content of Components in a Strain-Compensated Crystalline Ternary Alloy

A.Y. Nikulin, P. Zaumseil
Journal of Applied Physics **95**, 5249 (2004)

The x-ray Bragg diffraction intensity profile for a model strain-compensated structure consisting of a thin SiGe alloy layer grown on a thick Si substrate is derived using a Laplace transform interpretation of the kinematical approximation of x-ray diffraction theory. It is shown that in the case of fully strain-compensated crystals a simplified x-ray phase-retrieval technique can be applied to determine the alloy composition from this x-ray diffraction data. An experimental intensity profile from an almost perfectly unstrained SiGe: C/Si structure is analyzed using this method.

(16) Stability and Electronic Properties of Silicates in the System SiO₂-Pr₂O₃-Si(001)

D. Schmeißer, H.-J. Müssig
Journal of Physics Condensed Matter **16**, 153 (2004)

Pr_2O_3 is one of the most promising hetero-oxides that are the candidates of choice to replace SiO_2 as the gate dielectric material for sub-0.1 μm CMOS technology. In order to enable process integration, however, hetero-oxides require substantial characterization. In particular, the basic interaction mechanisms at the interface to the silicon substrate are the key issues. A solid knowledge of these mechanisms is required to address reliability arguments. The challenges in material science are to understand the chemical bonding of the hetero-oxides and Si on a microscopic scale. We report on the specific variations in the electronic structure which are evident in the valence band features around resonant excitation at the Pr 4d threshold. We also determine the valence band discontinuities at the $\text{Pr}_2\text{O}_3/\text{Si}(001)$ interface and follow the changes in the surface potentials to develop a band scheme, a prerequisite to understanding the properties of charge transport across that interface.

(17) Pr_2O_3 / Si(001) Interface Reactions and Stability

D. Schmeißer, J. Dabrowski, H.-J. Müssig
Materials Science and Engineering **B 109**, 30 (2004)

We show that an interfacial silicate is formed in a natural way between Si(001) and the deposited Pr_2O_3 film if a sufficient amount of oxygen is provided during deposition, as during electron beam evaporation from Pr_6O_{11} source. We provide arguments from results of *ab initio* calculations and we present a ternary phase diagram of the Pr-O-Si system obtained for epitaxial films from non-destructive depth profiling data acquired by synchrotron radiation and photo-electron spectroscopy (SR-PES) at the undulator beam line U49/2-PGM2. The composition of the interfacial layer is $(\text{Pr}_2\text{O}_3)_x(\text{SiO})_x(\text{SiO}_2)_y$ with $x+y$ between 2 and 6 and depends on the growth conditions and distance from the substrate. No interfacial SiO_2 and no interfacial silicide is formed during growth. The ternary phase diagram indicates that this non-stoichiometric pseudobinary alloy is stable on Si up to high temperatures, without phase separation into Pr_2O_3 and SiO_2 . Therefore, a complete re-engineering of the CMOS process may be not necessary.

(18) Silicate Layer Formation at $\text{Pr}_2\text{O}_3/\text{Si}(001)$ Interfaces

D. Schmeißer, H.-J. Müssig, J. Dabrowski
Applied Physics Letters **85**, 88 (2004)

We studied $\text{Pr}_2\text{O}_3/\text{Si}(001)$ interfaces by synchrotron radiation photoelectron spectroscopy and by *ab initio* calculations. We show that the interface formed during molecular-beam epitaxy under the oxygen partial pressure above 1×10^{-8} mbar consists of a mixed Si-Pr oxide, such as $(\text{Pr}_2\text{O}_3)_x(\text{SiO})_x(\text{SiO}_2)_y$. Neither an interfacial SiO_2 nor an interfacial silicide is formed. The silicate formation is driven by a low energy of O in a PrOSi bond and by the strain in the subsurface SiO_x layer. We expect that this natural interfacial Pr silicate will facilitate the integration of the high-*k* dielectric Pr_2O_3 into future complementary metal-oxide-semiconductor technologies.

(19) Pr_4f Occupancy and VB/CB Band Offsets of Pr_2O_3 at the Interface to Si (001) and SiC (0001) Surfaces

D. Schmeißer, H.-J. Müssig
Materials Science in Semiconductor Processing **7**, 221 (2004)

Resonant photoelectron spectroscopy (PES) at the Pr_{4d} and O1s absorption edges is used to study the electronic properties at the interface of epitaxially grown Pr_2O_3 on Si(001). In the electronic structure of bulk Pr_2O_3 , the valence band (VB) states are predominant of Pr_{6s} and O_{2p} atomic parentage. The contribution of Pr_{4f} states is identified from the strong increase of the VB features at the Pr_{4d} resonances. The data at the O1s edge are caused by Raman scattering and resonant Auger decay and reflect the existence of charge transfer (CT) complexes. These complexes are the consequence of a mixed valency caused by ligand-to- Pr_{4f} charge transfer states. The decrease of their intensity is attributed to an increase in covalent bandwidth between the ligand (O_{2p} , Si_{3p}) and Pr_{4f} states. The CT complexes, originally localized now, become broadened and form gap states which fill the gap towards a metallic density of states. The metallic phase may be hindered upon alloying with SiO_2 or other oxides.

(20) Structure and Thickness-dependent Lattice Parameters of Ultrathin Epitaxial Pr_2O_3 Films on Si(001) Studied by SR-GIXRD

T. Schröder, T.-L. Lee, J. Zegenhagen, C. Wenger, P. Zaumseil, H.-J. Müssig
Applied Physics Letters **85** (7), 1229 (2004)

Pr_2O_3 grown heteroepitaxially on Si(001) is a promising candidate for applications as a high-*k* dielectric

in future silicon-based microelectronics devices. The technologically important thickness range from 1 to 10 nm has been investigated by synchrotron radiation-grazing incidence x-ray diffraction. The oxide film grows as cubic Pr_2O_3 phase with its (101) plane on the Si (001) substrate in form of two orthogonal rotation domains. Monitoring the evolution of the oxide unit-cell lattice parameters as a function of film thickness from 1 to 10 nm, the transition from almost perfect pseudomorphism to bulk values is detected.

(21) Formation of Heavily P-doped Si Epitaxial Films on Si(100) by Multiple Atomic-Layer Doping Technique

Y. Shimamune, M. Sakuraba, J. Murota, B. Tillack
Applied Surface Science **224** (1-4), 202 (2004)

Phosphorus (P) incorporation process during Si epitaxial growth by SiH_4 reaction in ultraclean low-pressure chemical vapor deposition (CVD) and the electrical characteristics of the heavily P-doped epitaxial Si film on Si(100) have been investigated. Si layer growth on the P layer formed on Si(100) at 500°C at SiH_4 partial pressure of 6 Pa is observed when the surface P amount becomes below $7 \times 10^{14} \text{ cm}^{-2}$. It is also found that about $1.1 \times 10^{14} \text{ cm}^{-2}$ P atoms segregate onto the Si surface and the other desorbs. On the other hand, by lowering the Si growth temperature to 450°C and increase in the SiH_4 partial pressure to 220 Pa, P incorporation occurs and about $1.5 \times 10^{14} \text{ cm}^{-2}$ P atoms are buried at the initial position without segregation. By using the multiple atomic-layer doping technique, very low-resistive heavily P-doped epitaxial Si film on Si(100) can be formed with effective suppression of the electrically inactive P formation.

(22) High Performance SiGe:C HBTs Using Atomic Layer Base Doping

B. Tillack, Y. Yamamoto, D. Knoll, B. Heinemann, P. Schley, B. Senapati, D. Krüger
Applied Surface Science **224**, 55 (2004)

We applied atomic layer processing for base doping of high performance SiGe:C heterojunction bipolar transistors (HBTs) fabricated within a 0.25 mm BiCMOS technology. B atomic layer doping (ALD) was performed at 400°C during an interruption of the epitaxial SiGe:C base layer deposition. Atomic level dopant location and dose control was achieved. Electrical pro-

perties of atomic layer and box-profile doped (standard) HBTs were compared, showing peak f_T and f_{max} for the ALD HBT of 113 and 127 GHz, and of 108 and 123 GHz for the standard HBT, respectively. The internal base sheet resistances (RSBi) for the ALD and standard HBTs were comparable, indicating very similar active B dose for both doping variants. The HBT results demonstrate the capability of atomic layer processing for doping of advanced devices, with critical requirements for dose and location control.

(23) Recombination Activity and Electrical Levels of Dislocations in p-type SiGe Structures: Impact of Copper Contamination and Hydrogenation

O.F. Vyvenko, M. Kittler, W. Seifert
Journal of Applied Physics **96** (11), 6425 (2004)

The impact of copper contamination and subsequent hydrogenation on recombination activity and hole-trap levels of misfit dislocations were investigated in p-type Si/Si_{0.98}Ge_{0.02}/Si structures. In the as-grown (noncontaminated) samples, dislocations were found to exhibit very low recombination activity, detectable with the electron-beam-induced current technique only at low temperatures. Deep-level transient spectroscopy revealed a dislocation-related hole-trap level at $E_t = E_v + 0.2 \text{ eV}$. The position of the observed level is close to the theoretically predicted hole-trap state of the intrinsic stacking fault of a dissociated dislocation. Contamination with a low copper concentration [5 (parts per 10⁹) ppb] gave rise to a large increase of the recombination activity of the dislocations and to the appearance of another dislocation-related defect level at $E_t = E_v + 0.32 \text{ eV}$. Hydrogenation of the samples by a treatment with an acid solution and subsequent reverse-bias anneal at 380 K resulted in the evolution of the levels of substitutional copper and its complexes with hydrogen.

(24) First Investigation of MIM Capacitors Using Pr₂O₃ Dielectrics

C. Wenger, J. Dabrowski, P. Zaumseil, R. Sorge, P. Formanek, G. Lippert, H.-J. Müssig
Materials Science in Semiconductor Processing **7** (4-6), 227 (2004)

Metal-insulator-metal (MIM) capacitors with Pr_2O_3 as high-k material have been investigated for the first time. We varied the thickness of the Pr_2O_3 layers as well as the bottom electrode material. The layers are

characterised using X-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD), transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS). Preliminary information on the interaction of water with the films was obtained from XPS and ab initio pseudopotential calculations. The electrical characterisation shows that Pr_2O_3 MIM capacitors can provide higher capacitance densities than Si_3N_4 MIM capacitors while still maintaining comparable voltage coefficients of capacitance. The Pr_2O_3 dielectric material seems to be suitable for use in silicon RF applications.

(25) Circuit Applications of High-Performance SiGe:C HBTs Integrated in BiCMOS Technology

W. Winkler, J. Borngräber, B. Heinemann, H. Rücker, R. Barth, J. Bauer, D. Bolze, E. Bugiel, J. Drews, K.-E. Ehwald, T. Grabolla, U. Haak, W. Höppner, D. Knoll, D. Krüger, B. Kuck, R. Kurps, S. Marschmeyer, H.H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, D. Wolansky, H.-E. Wulf, Y. Yamamoto, P. Zaumseil
Applied Surface Science **224** (1-4), 297 (2004)

Carbon-doped SiGe (SiGe:C) bipolar devices have been developed and integrated in to a 0.25 μm CMOS platform. The resulting SiGe:C BiCMOS technology offers a wide spectrum of active and passive devices for wireless and wired communication systems. A high-performance variant of the bipolar transistor has been derived from the standard transistors by reduction of some transistor dimensions. With these alterations, f_T and f_{max} of the bipolar transistors reaches 120 and 140 GHz, respectively. Circuit applications of the devices are demonstrated. Static and dynamic divider circuits have a maximum input frequency of 62 and 72 GHz, respectively. Integrated LC oscillators with frequencies up to 60 GHz are also demonstrated.

(26) Carbon and Boron in Heavily Doped SiGe:C/Si Epilayers Studied by FTIR

V.D. Akhmetov, O. Lysytskiy, Y. Yamamoto, H. Richter
Electrochemical Society Proceedings **Vol. 2004-07**, 269 (2004)

(27) Nitrogen in Thin Silicon Wafers Determined by Infrared Spectroscopy

V.D. Akhmetov, O. Lysytskiy, H. Richter
Electrochemical Society Proceedings **Vol. 2004-05**, 109 (2004)

(28) HICUM Modeling of SiGe-HBTs Fabricated in Wafer Bonded SOI Substrates

A. Chakravorty, B. Senapati, G. Dalapati, R. Garg, C.K. Maiti, G.A. Armstrong, H.S. Gamble, P. Ashburn and H.A.W. El Mubarek
Proc. International Conference on Computers and Devices for Communication, **42** (2004)

(29) Accurate Modeling of SiGe:C HBTs using Adaptive Neuro-Fuzzy Inference System

A. Chakravorty, R.F. Scholz, B. Senapati, D. Knoll, A. Fox, R. Garg, C.K. Maiti
Proc. ISTDM, **264** (2004)

(30) Electrical Deactivation and Diffusion of Boron in Preamorphized Ultrashallow Junctions: Interstitial Transport and F co-implant Control

B. Colombeau, A.J. Smith, N.E.B. Cowern, W. Lerch, S. Paul, B.J. Pawlak, F. Christiano, X. Hebras, D. Bolze, C. Ortiz, P. Pichler
Technical Digest IEDM, **971** (2004)

(31) Preface

J. Dabrowski, H.-J. Müssig
Materials Science in Semiconductor Processing **7** (4-6), 165 (2004)

(32) Ab Initio Study of Pr Oxides for CMOS Technology

J. Dabrowski, V. Zavodinsky
Proc. NIC Symposium, **171** (2004)

(33) Transistors and Atoms

J. Dabrowski, H.-J. Müssig, E.R. Weber, W. Schröter
Challenges in Process Simulation / ed. by J. Dabrowski, E.R. Weber, Berlin, Springer Verlag, **1-38** (2004)

(34) Model-driven Design of the WIN Platform

J. deMeer
Proc. ICSSEA, ISSN: 1637-5033, **Vol. 3** (2004)

(35) High-Level Behavioral SDL Model for the IEEE 802.15.3. MAC Protocol

D. Dietterle, I. Babanskaja, K. Dombrowski, R. Kraemer
Proc. WWIC 2004, Febr. 05-07, 2004, Frankfurt (Oder), Germany. - Berlin, Springer, **165** (2004)

- (36) **Mapping of High-Level SDL Models to Efficient Implementations for TinyOS**
D. Dietterle, J. Ryman, K. Dombrowski, R. Kraemer
Proc. EUROMICRO Symposium on Digital System Design, IEEE Computer Society, **402** (2004)
- (37) **A Two Mask Complementary LDMOS Module Integrated in a 0.25 μm SiGe:C BiCMOS Platform**
K.-E. Ewald, A. Fischer, F. F \ddot{u} rnhammer, W. Winkler, B. Senapati, R. Barth, D. Bolze, B. Heinemann, D. Knoll, H. R \ddot{u} cker, D. Schmidt, I. Shevchenko, R. Sorge, H.-E. Wulf
Proc. ESSDERC, **121** (2004)
- (38) **Bluetooth Indoor Localization System**
G. Fischer, B. Dietrich, F. Winkler
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- (40) **Spectroscopic Ellipsometry for In-Line Process Control of SiGe:C HBT Technology**
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- (41) **A DC – 10 GHz Amplifier With Digital Offset Correction**
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- (42) **A Fully-Integrated Low-Power Low-Jitter Clock Synthesizer with 1.2 GHz Tuning Range in SiGe:C BiCMOS**
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- (43) **Complementary SiGe BiCMOS**
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- (44) **A Low-Parasitic Collector Construction for High-Speed SiGe:C HBTs**
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- (45) **Jitter and Phase-Noise in Oscillators and Phase-Locked Loops**
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- (46) **Standardization of Defect Characterization Technique in Annealed CZ Si**
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- (62) **Applying Position Prediction as a Means for Performance-Tuning in Location-Aware Platforms**
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- (63) **Moneta: An Anonymity Providing Lightweight Payment System for Mobile Devices**
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- (64) **Ensuring Anonymity in e-commerce Systems Using a Hidden Identity Approach: Discussion of Problems and Solutions**
K. Piotrowski, P. Langendörfer, O. Maye
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- (65) **SiGe HBT Design for High-Frequency Applications**
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- (66) **Advances in SiGe HBT Technology in Europe**
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- (67) **Integration of High-Performance SiGe:C HBTs with Thin-Film SOI CMOS**
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- (69) **Analysis of Microwave Noise Sources in 150 GHz SiGe HBTs**
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- (70) **A 1 GHz AGC Amplifier in BiCMOS with 3µs Settling-Time for 802.11a WLAN**
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- (71) **Advanced Technique for Broadband on-Wafer RF Device Characterization**
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- (72) **Macro Model of Power RF LDMOSFET**
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- (73) **Application of the VBIC Model for SiGe:C Heterojunction Transistors**
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- (74) **Self-Consistent Characterization of Gate Controlled Diodes for CMOS Technology Monitoring**
R. Sorge, P. Schley, K.-E. Ehwald
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- (75) **Modular Processor: A Flexible Library of ASIC Modules**
Z. Stamenkovic, G. Panic, U. Jagdhold, H. Frankenfeldt, K. Tittelbach-Helmrich, G. Schoof, R. Kraemer
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- (76) **Atomic Level Control of SiGe Epitaxy and Doping**
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- (77) **A 117 GHz LC-Oscillator in SiGe:C BiCMOS Technology**
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- (78) **LC-Oscillators Above 100 GHz in Silicon-Based Technology**
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(79) High-Frequency Low-Noise Amplifiers and Low-Jitter Oscillators in SiGe:C BiCMOS Technology

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(80) 60 GHz Transceiver Circuits in SiGe:C BiCMOS Technology

W. Winkler, J. Borngräber, F. Herzel, H. Gustat, B. Heinemann, F. Korndörfer
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Eingeladene Vorträge Invited Presentations

(1) Determination of Optical Constants Using Swing Curves

J. Bauer, U. Haak, G. Drescher
Lithography Workshop, Pommelsbrunn, September 17-19, 2004, Germany

(2) Mobile Application Patterns – Real Time or Ubiquity?

J. deMeer
UML/Java Workshop für Embedded und Real-time Systeme, TFH Berlin, July 29, 2004, Germany

(3) Presentations of the IHP PLASMA Platform

J. deMeer, R. Kraemer
Visit of the Middleware Research Labs – Toronto, Montreal, Nashville, March 27 – April 4, 2004, Canada and USA

(4) MEDman – Ubiquitous Medical Assistance

J. deMeer
EUREKA MEDEA+ Board Paris, May 25 and June 3, 2004, France

(5) Mobile Nutzung von Sensornetzwerken auf der PLASMA-Plattform

J. deMeer, P. Langendörfer
Ringvorlesung des Instituts für Informatik und Gesellschaft der Universität Freiburg (Breisgau), June 28, 2004, Germany

(6) Mobile Nutzung von Sensornetzwerken auf der PLASMA-Plattform

J. deMeer, P. Langendörfer
Colloquium des Fachbereichs Informatik der Universität Passau, June 29, 2004, Germany

(7) Analog Design Challenges in Ultrawide-Band Technology

B. Dietrich
International Union of Radio Science, Landesausschuss in der Bundesrepublik Deutschland, Kleinheubacher Tagung Miltenberg, September 24, 2004, Germany

(8) Complementary SiGe BiCMOS

B. Heinemann, J. Drews, D. Knoll, R. Kurps, S. Marschmeyer, H. Rücker, W. Winkler, Y. Yamamoto
SiGe: Materials, Processing, and Devices : The 1st International Symposium, Honolulu, October 03-08, 2004, Hawaii, USA

(9) BiCMOS Integration of High-Speed SiGe:C HBTs

B. Heinemann, H. Rücker
Workshop Advances in Modeling and Simulation of Semiconductor Devices, Berlin, July 12-16, 2004, Germany

(10) Silicon-based Light Emission After Ion Implantation: Role of Defects and of Crystalline Perfection

M. Kittler
10th Internat. Conf. on "Extended Defects in Semiconductors" EDS 2004, Moscow, September 2004, Russia

(11) Si-basierte Lichtemitter für die On-chip-Datenübertragung

M. Kittler
FhG Inst. für Photonische Mikrosysteme, Dresden, October 7, 2004, Germany

(12) Energy Efficient Middleware Design in Support of User Privacy

P. Langendörfer
Panel Discussion at 4th Workshop on Applications and Services in Wireless Networks, Boston, August 09-11, 2004, USA

- (13) **PLASMA: A Location-, Privacy- and Energy-aware Middleware Platform**
P. Langendörfer
North Eastern University, Boston, August 12, 2004, USA
- (14) **Are There Alternatives to Silicon Based Technology**
W. Mehr
EMRS 2004 Spring Meeting Strasbourg, May 26, 2004, France
- (15) **Mikroelektronik – der große Schritt in kleinste Welten**
W. Mehr
Tag der Wissenschaft an der Europa-Universität Frankfurt (Oder), November 10, 2004, Germany
- (16) **Alternative SOI-Strukturen**
H.-J. Müssig
Siltronic AG Burghausen, March 25, 2004, Germany
- (17) **Neue Materialien in der Mikroelektronik – Trends und Anforderungen**
H.-J. Müssig
Institut für Ionenstrahlphysik und Materialforschung Forschungszentrum Rossendorf, March 29, 2004, Germany
- (18) **Welche Rolle spielen neue Materialien in der Mikroelektronik?**
H.-J. Müssig
Tag der offenen Tür im IHP, Frankfurt (Oder), September 04, 2004, Germany
- (19) **Atomically Controlled Impurity Doping in Si-Based CVD**
J. Murota, M. Sakuraba, B. Tillack
MRS Spring Meeting 2004, San Francisco, April 12-16, 2004, USA
- (20) **IHP – Institut für innovative Mikroelektronik**
H. Richter
Hochschulinformationstag der TFH Wildau, May 7, 2004, Germany
- (21) **Defect Engineering und Wafer Design in der Siliziumtechnologie**
H. Richter
Freiburger Materialforschungszentrum, Freiburg, July 9, 2004, Germany
- (22) **Si Crystal Growth and Defect Engineering**
H. Richter
The 4th Int. Symp. On Advanced Science and Technology of Silicon Materials, Kona, Hawaii, November 22-26, 2004, USA
- (23) **SiGe HBT Design for High-Frequency Applications**
H. Rücker, B. Heinemann, R. Barth, D. Knoll, P. Schley, R. Scholz, B. Tillack, W. Winkler
2nd ISTDM 2004, Frankfurt (Oder), May 16-19, 2004, Germany
- (24) **Advances in SiGe HBT Technology in Europe**
H. Rücker, W. Winkler
Compound Semiconductor IC Symposium, Monterey, October 23-28, 2004, USA
- (25) **A Comparative SR-GIXRD, STM and LEED Study of the Structural Properties of Pr₂O₃ Epilayers on Si(001) and Si(111)**
T. Schröder, H.-J. Müssig
Hahn Meitner Institute Berlin, April 2004, Germany
- (26) **Modern Synchrotron Radiation Grazing Incidence Diffraction Studies: The Example of Epitaxial Pr₂O₃ Layers on Si(001) and Si(111)**
T. Schröder, T.L. Lee, L. Libralesso, J. Zegenhagen, C. Wenger, P. Zaumseil, H.-J. Müssig
Ecole Centrale de Lyon, Laboratory of Electronical Engineering, Lyon, July 2004, France
- (27) **Atomic Level Control of SiGe Epitaxy and Doping**
B. Tillack
University of Hannover, Institute for Semiconductor Devices and Electronic Materials, July 8, 2004, Germany

- (28) **High-Performance, Low-Cost SiGe:C BiCMOS Technology**
B. Tillack, D. Knoll, B. Heinemann, K.-E. Ewald, H. Rücker, R. Barth, P. Schley, W. Winkler
Semicon Europe, Munich, April 20-22, 2004, Germany
- (29) **High-Performance, Low-Cost SiGe:C BiCMOS Technology**
B. Tillack, D. Knoll, B. Heinemann, K.-E. Ewald, H. Rücker, R. Barth, P. Schley, W. Winkler
STS Session: SiGe/SOI/Strained Si: From Growth to Device Properties, International Congress Center Munich, April 21, 2004, Germany
- (30) **Atomic Level Control of SiGe Epitaxy and Doping**
B. Tillack, Y. Yamamoto, J. Murota
SiGe: Materials, Processing, and Devices: The 1st International Symposium, Honolulu, October 03-08, 2004, Hawaii, USA
- (31) **Application of SiGe:C BiCMOS to Wireless and Radar**
W. Winkler, B. Heinemann, D. Knoll
European Gallium Arsenide and other Compound Semiconductors Application Symposium, Amsterdam, October 11-12, 2004, The Netherlands
- (32) **High Resolution X-Ray Characterization of SiGe:C Structures for High Frequency Microelectronics Applications**
P. Zaumseil
HREDAMM, Zakopane, June 13-17, 2004, Poland
- (2) **Carbon and Boron in Heavily Doped SiGe:C/Si Epilayers Studied by FTIR**
V.D. Akhmetov, O. Lysytskiy, Y. Yamamoto, H. Richter
SiGe: Materials, Processing, and Devices: The 1st International Symposium, Honolulu, October 03-08, 2004 Hawaii, USA
- (3) **Silicon-based Light Emission after Ion Implantation**
T. Arguirov, M. Kittler, W. Seifert, A. Fischer
9th Augustusburg Conference of Advanced Science, Das Silicium-Zeitalter: Silicium für Mikroelektronik, Photovoltaik und Photonik, Augustusburg, September 23-25, 2004, Germany
- (4) **Bestimmung der optischen Eigenschaften des Fotoresists für die Fotolithographie-Wellenlängen durch Swingoptimierung**
J. Bauer, U. Haak, G. Drescher
3rd Workshop Ellipsometrie, Stuttgart, February 23-25, 2004, Germany
- (5) **Effects of Various Ci/Ti and Co/TiN Layer Stacks and the Silicide Rapid Thermal Process Conditions on Cobalt Silicide Formation**
S. Buschbaum, O. Fursenko, D. Bolze, D. Wolansky, V. Melnik, J. Nieß, W. Lerch
MAM 2004 – Materials for Advanced Metallization, Brussels, March 2004, Belgium
- (6) **Accurate Modeling of SiGe:C HBTs using Adaptive Neuro-Fuzzy Inference System**
A. Chakravorty, R.F. Scholz, B. Senapati, D. Knoll, A. Fox, R. Garg, C.K. Maiti
2nd ISTDM 2004, Frankfurt (Oder), May 16-19, 2004, Germany
- (7) **Electrical Deactivation and Diffusion of Boron in Preamorphized Ultrashallow Junctions: Interstitial Transport and F co-implant Control**
B. Colombeau, A.J. Smith, N.E.B. Covern, W. Lerch, S. Paul, B.J. Pawlak, F. Christiano, X. Hebras, D. Bolze, C. Ortiz, P. Pichler
IEDM 2004, San Francisco, December 13-15, 2004, USA

Vorträge

Presentations

- (1) **Nitrogen in Thin Silicon Wafers Determined by Infrared Spectroscopy**
V.D. Akhmetov, O. Lysytskiy, H. Richter
9th Augustusburg Conference of Advanced Science, Das Silicium-Zeitalter: Silicium für Mikroelektronik, Photovoltaik und Photonik, Augustusburg, September 23-25, 2004, Germany

- (8) **MEDman – Ubiquitous Medical Assistance**
J. deMeer
EUREKA MEDEA+ Board Paris, June 03, 2004, France
- (9) **Model-driven Design of the WIN Platform**
J. deMeer
17^{èmes} Journées Internationales «Génie Logiciel & Ingénierie de Systèmes et leurs Applications», Paris – November 30 - December 2, 2004, France
- (10) **How to Achieve Security by Architecturing Middleware Supporting Mobile Applications**
J. deMeer
IST 2004 Conference – Workshop on Emerging Security Technology, Den Haag, November 15-17, 2004, The Netherlands
- (11) **Deployment of Sensor Networks to medical and other Business Application Domains**
J. deMeer
IST 2004 Conference – Workshop on Research Collaboration between Canada and Europe, Den Haag, November 15-17, 2004, The Netherlands
- (12) **High-Level Behavioral SDL Model for the IEEE 802.15.3 MAC Protocol**
D. Dietterle, I. Babanskaja, K. Dombrowski, R. Kraemer
WWIC 2004, Frankfurt (Oder), February 05-07, 2004, Germany
- (13) **Mapping of High-Level SDL Models to Efficient Implementations for TinyOS**
D. Dietterle, J. Ryman, K. Dombrowski, R. Kraemer
EUROMICRO Symposium on Digital System Design, Rennes, August 31- September 03, 2004, France
- (14) **Integrated RF LDMOS**
K.-E. Ehwald
Workshop High-Performance SiGe:C BiCMOS for Wireless and Broadband Communication, Frankfurt (Oder), September 30, 2004, Germany
- (15) **A Two Mask Complementary LDMOS Module Integrated in a 0.25 μm SiGe:C BiCMOS Platform**
K.-E. Ehwald, A. Fischer, F. Föhnhammer, W. Winkler, B. Senapati, R. Barth, D. Bolze, B. Heinemann, D. Knoll, H. Rücker, D. Schmidt, I. Shevchenko, R. Sorge, H.-E. Wulf
ESSDERC 2004, Leuven, September 21-23, 2004, Belgium
- (16) **Bluetooth Indoor Localization System**
G. Fischer, B. Dietrich, F. Winkler
1st Workshop on Positioning, Navigation and Communication 2004, Hannover, March 26, 2004, Germany
- (17) **SiGe:C-BiCMOS-Technologie als Basis für UWB-Transceiver**
G. Fischer, B. Heinemann, R. Kraemer
Öffentliche Diskussionsitzung des Fachausschusses 7.2 der ITG zu Ultra Wide Band – Technologien und mögliche Anwendungen, Kamp-Lintfort, November 11, 2004, Germany
- (18) **Application of Electron Holography in BiCMOS Technology**
P. Formanek, B. Heinemann, M. Kittler, D. Krüger, R. Kurps, A. Orchowski, A. Ourmazd, W.-D. Rau, H. Rücker, P. Schwander, B. Tillack, P. Zaumseil
2nd ISTDM 2004, Frankfurt (Oder), May 16-19, 2004, Germany
- (19) **Application of Electron Holography to Extended Defects: Schottky Barriers at NiSi₂ Precipitates in Silicon**
P. Formanek, M. Kittler
10th Internat. Conf. on Extended Defects in Semiconductors – EDS 2004, Moscow, September, 2004, Russia
- (20) **Flash Integration**
A. Fox
Workshop High-Performance SiGe:C BiCMOS for Wireless and Broadband Communication, Frankfurt (Oder), September 30, 2004, Germany
- (21) **Cost-effective Integration of an FN-programmed Embedded Flash Memory into a 0.25 μm RF-BiCMOS Technology**
A. Fox, K.-E. Ehwald, P. Schley, R. Barth, S. Marschmeyer, V.E. Stikanov, A. Gromovyy, A. Hudryyev
The ICM 2004 International Conference on Microelectronics, Tunis, December 6-8, 2004, Tunisia

- (22) **Optimization of Anti-reflective Coating PECVD SiO_xN_y for Lithography Application**
O. Fursenko, J. Bauer, B. Kuck, A. Penkov
3rd Workshop Ellipsometrie, Stuttgart, February 23-25, 2004, Germany
- (23) **Spectroscopic Ellipsometry for In-Line Process Control of SiGe:C HBT Technology**
O. Fursenko, J. Bauer, P. Zaumseil, D. Krüger, A. Goryachko, Y. Yamamoto, K. Köpke, B. Tillack
2nd ISTDM 2004, Frankfurt (Oder), May 16-19, 2004, Germany
- (24) **A DC – 10 GHz Amplifier With Digital Offset Correction**
H. Gustat
2nd ISTDM 2004, Frankfurt (Oder), May 16-19, 2004, Germany
- (25) **A Fully-Integrated Low-Power Low-Jitter Clock Synthesizer with 1.2 GHz Tuning Range in SiGe:C BiCMOS**
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2nd ISTDM 2004, Frankfurt (Oder), May 16-19, 2004, Germany
- (26) **A Low-Parasitic Collector Construction for High-Speed SiGe:C HBTs**
B. Heinemann, R. Barth, D. Bolze, J. Drews, P. Formanek, T. Grabolla, U. Haak, W. Höppner, D. Knoll, B. Kuck, R. Kurps, K. Köpke, S. Marschmeyer, H.H. Richter, H. Rücker, P. Schley, D. Schmidt, W. Winkler, D. Wolansky, H.-E. Wulf, Y. Yamamoto
IEDM 2004, San Francisco, December 13-15, 2004, USA
- (27) **High-performance HBT Modules in BiCMOS**
B. Heinemann
Workshop High-Performance SiGe:C BiCMOS for Wireless and Broadband Communication, Frankfurt (Oder), September 30, 2004, Germany
- (28) **Jitter and Phase-Noise in Oscillators and Phase-locked Loops**
F. Herzel, W. Winkler, J. Borngräber
2nd International Symposium on Fluctuations and Noise, Maspalomas, Gran Canaria, May 26-28, 2004, Spain
- (29) **Standardization of Defect Characterization Technique in Annealed CZ Si**
N. Inoue, K. Moriya, K. Kashima, R. Takeda, V.D. Akhmetov, O. Lysytshiy, K. Nakashima
4th International Symposium on Advanced Science and Technology of Silicon Materials, Kona, November 22-26, 2004, USA
- (30) **Oxygen, Nitrogen, Intrinsic Point Defects and their Interaction in Defect Generation for Internal Gettering**
G. Kissinger
Physikalisches Kolloquium der BTU Cottbus, November 11, 2004, Germany
- (31) **Direct Evidence of Internal Schottky Barriers at NiSi₂ Precipitates in Si by Electron Holography**
M. Kittler
Gordon Conference on Defects in Semiconductors, New London, July 2004, USA
- (32) **Raumladung an NiSi₂-Präzipitaten in n-Si**
M. Kittler, P. Formanek
Arbeitsreffen ASIS-Verbundprojekt, Grosse Leder, April 2004, Germany
- (33) **Silicon-based Light Emission after Ion Implantation**
M. Kittler, T. Arguirov, A. Fischer, W. Seifert
E-MRS Spring Meeting 2004, Strasbourg, May 24-28, 2004, France
- (34) **Silicon-based Light Emission After Ion Implantation**
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(10) Verfahren zum schrittweisen Austausch persönlicher Informationen in non-trusted Peer-to-Peer Umgebungen

T. Falck, H. Maaß, K. Weidenhaupt, P. Langendörfer
PHDE30356, PCT-Anmeldung mit Philips

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